Patent claims

1. An electronic component with a housing package (2) comprising a number of layers of plastic (3), with at least one buried interconnect layer (4) and with at least one semiconductor chip (5), which has pointed-conical external contacts (7) distributed on an outer side (6), the pointed-conical external contacts (7) penetrating through one of the layers of plastic in the housing package and forming contact vias to the buried interconnect layer (4).

2. The electronic component according to claim 1, characterized in that the electronic component (1) is a multichip module (9) with a number of buried interconnect layers (4) and a number of semiconductor chips (5) which have pointed-conical external contacts (7), the pointed-conical external contacts (7) of the semiconductor chips (5) in the housing package (2) penetrating through different layers of plastic (3) and forming contact vias (8) with respect to different buried interconnect layers (4).

3. The electronic component according to claim 1 or claim 2, characterized in that the electronic component (1) has buried semiconductor chips (10).

4. The electronic component according to one of the preceding claims, characterized in that the electronic component (1) has thinned semiconductor chips (11) with a thickness of between 30 and 100 micrometers as buried semiconductor chips (10).

5. The electronic component according to one of claims 2 to 4, characterized in that the multichip module (9) has external contact areas (14) on the underside (12) and/or the upper side (13).

6. The electronic component according to one of claims 2 to 5, characterized in that the multichip module (9) has semiconductor chips (5) on its upper side (13), the chips penetrating with their pointed-conical external contacts (7) through the uppermost layer of plastic (15) and forming contact vias (8) to a buried interconnect layer (4).

7. The electronic component according to one of claims 2 to 6, characterized in that the multichip module (9) has passive components (16) on its upper side (13), the components being connected by means of contact vias (8) in the uppermost layer of plastic (15) to one of the buried interconnect layers (4).

8. The electronic component according to one of the preceding claims, characterized in that a hollow housing package (17) has the layers of plastic (3), the buried interconnect layer (4) and the at least one semiconductor chip (5), one of the layers of plastic (3) forming a covering (18) with contact vias (8) and a further layer of plastic (3) comprising the frame (19) of the hollow housing package (17), which is penetrated by the pointed-conical external contacts (7) of the semiconductor chip (5), the pointed-conical external contacts (7) being electrically connected to contact vias (8) of the covering (18).

9. The electronic component according to claim 8, characterized in that the hollow housing package (17) is a light sensor housing or chip camera housing and the covering (18) has a transparent layer of plastic (20).

10. The electronic component according to claim 8 or claim 9, characterized in that the hollow housing

package (17) is a pressure sensor housing and the covering (18) has a central opening (21) for pressure coupling.

11. The electronic component according to one of claims 8 to 10, characterized in that the hollow housing package (17) is a gas sensor housing and the covering (18) has a central opening (21) for gas exchange.

12. The electronic component according to one of claims 8 to 11, characterized in that the hollow housing package (17) is a sound sensor housing and the covering (18) has a central opening (21) for receiving sound or emitting sound.

13. The electronic component according to one of the preceding claims, characterized in that at least one of the layers of plastic (3) has a pre-crosslinked plastic (22).

14. The electronic component according to one of the preceding claims, characterized in that at least one of the layers of plastic (3) has glass fiber or carbon fiber reinforcements.

15. A panel with a number of component positions (23), the panel (24) comprising a number of layers of plastic (3) and at least one buried interconnect layer (4), and each component position (23) having at least one semiconductor chip (5) with pointed-conical external contacts (7) distributed on an outer side (6), and the pointed-conical external contacts (7) in the panel (24) penetrating through one of the layers of plastic (3) and forming contact vias (8) to the buried interconnect layer (4).

16. The panel according to claim 15, characterized in that each component position (23) comprises a multichip module (9) with a number of buried interconnect layers (4) and a number of semiconductor chips (5), which have pointed-conical external contacts (7), the pointed-conical external contacts (7) of the semiconductor chips (5) penetrating through different layers of plastic (3) in the panel (24) and forming contact vias (8) to different buried interconnect layers (4).

17. The panel according to claim 15 or claim 16, characterized in that the panel (24) has buried semiconductor chips (10).

18. The panel according to one of claims 15 to 17, characterized in that the panel (24) has thinned semiconductor chips (11) with a thickness of between 30 and 100 micrometers as buried semiconductor chips (10).

19. The panel according to claims 15 to 18, characterized in that the panel (24) has external contact areas (14) in each component position (23) on the underside (12) and/or the upper side (13).

20. The panel according to claims 15 to 19, characterized in that the panel (24) has semiconductor chips (5) in each component position (23) on its upper side (13), the chips penetrating with their pointed-conical external contacts (7) through the uppermost layer of plastic (15) and forming contact vias (8) to a buried interconnect layer (4).

21. The panel according to claims 15 to 20, characterized in that the panel (24) has passive components (16) on its upper side (13), the

components being connected by means of contact vias (8) in the uppermost layer of plastic (15) to one of the buried interconnect layers (4).

22. The panel according to one of claims 15 to 21, characterized in that the panel (24) has in one of the layers of plastic (3) a depression for a hollow housing package (17) in each component position (23), with at least one buried interconnect layer (4) and with at least one semiconductor chip (5), a further one of the layers of plastic (3) forming a covering (18) with contact vias (8).

23. The panel according to one of claims 15 to 22, characterized in that the panel (24) has at least one layer of plastic (3) of a pre-crosslinked plastic (22).

24. The panel according to one of claims 15 to 23, characterized in that the panel (24) has at least one layer of plastic (3) with glass fiber or carbon fiber reinforcements.

25. A method for producing at least one electronic component (1) with a housing package (2) comprising a number of layers of plastic (3), with at least one buried interconnect layer (4) and with at least one semiconductor chip (5), which has pointed-conical external contacts (7) disposed on an outer side (6), the pointed-conical external contacts (7) penetrating through one of the layers of plastic (3) in the housing package (2) and forming contact vias (8) to the buried interconnect layer (4), the method comprising the following method steps:

- production of a circuit carrier (26) with external contact areas (14) on the underside (12) of the circuit carrier (26) and an interconnect layer (4) on the upper side (27) of the circuit

carrier (26), the external contact areas (14) and the interconnect layer (4) being electrically connected by means of contact vias (8) through the circuit carrier (26),

- production of semiconductor chips (5) with pointed-conical external contacts (7),
- application of a pre-crosslinked layer of plastic (22) to the interconnect layer (4) of the circuit carrier (26),
- penetration of the pre-crosslinked layer of plastic (22) with the pointed-conical external contacts (7) of at least one of the semiconductor chips (5) until the pointed-conical external contacts (7) form contact vias (8) to the interconnect layer and the at least one semiconductor chip (5) is impressed in the pre-crosslinked layer of plastic (22),
- curing and crosslinking of the pre-crosslinked layer of plastic (22) to form a layer of plastic (3),
- functional testing of the electronic component (1) by means of the external contact areas (14) of the circuit carrier (26).

26. The method according to claim 25, characterized in that, before the curing and crosslinking of the pre-crosslinked layer of plastic (22), a further pre-crosslinked layer of plastic (22) is applied to cover the semiconductor chip (5).

27. The method according to claim 25 or claim 26, characterized in that a structured pre-crosslinked layer of plastic (22) with at least one depression (25) for a hollow housing package (17) is applied to the interconnect layer (4) of the circuit carrier (26).

28. The method according to one of claims 25 to 27, characterized in that a number of sequences of interconnect layers (4) and layers of plastic (3) with contact vias (8) and embedded semiconductor chips (10) are applied to the interconnect layer (4) of the circuit carrier (26), the pointed-conical external contacts (7) of the semiconductor chip (5) respectively penetrating through one of the layers of plastic (3) and forming contact vias (8) to one of the interconnect layers (4).

29. The method according to one of claims 25 to 28, characterized in that an upper interconnect layer (4), which is loaded with semiconductor chips (5) and/or passive components (16) to form a multichip module (9), is applied to an uppermost layer of plastic (15).

30. The method according to one of claims 25 to 29, characterized in that the claimed method steps for producing a panel (24) with a number of component positions (23) are carried out and the panel (24) is finally divided up into individual electronic components (1).